REMARKS

Applicants appreciate the Examiner's thorough examination of the present application as evidenced by the Office Action of March 26, 2004 (hereinafter "Office Action"). In response, Applicants respectfully submit that the cited reference does not disclose or suggest all of the recitations of the independent claims. Accordingly, Applicants submit that all pending claims are in condition for allowance. Favorable reconsideration of all pending claims is respectfully requested for at least the reasons discussed hereafter.

Independent Claims 1, 14, 19 are Patentable

Independent Claims 1, 14, and 19 stand rejected under 35 U.S.C. §102(b) as being anticipated by U. S. Patent No. 5,940,608 to Manning (hereinafter "Manning").

Independent Claim 1 is directed to a clock distribution circuit that comprises both a first and a second clock circuit that are each responsive to an error signal as indicated by the recitations of Claim 1 reproduced in part below:

> a first clock circuit that is configured to generate a first clock signal responsive to an error signal;
>
> a second clock circuit that is configured to generate a second clock signal responsive to the error signal; (emphasis added)
>
> ...

Independent Claim 8 is directed to a clock distribution circuit that comprises a plurality of clock circuits that are responsive to respective ones of a plurality of error signals as indicated by the recitations of Claim 8 reproduced in part below:

> ...
>
> a plurality of clock circuits, respective ones of the plurality of clock circuits being directly connected to at least one other of the plurality of clock circuits by respective ones of the plurality of phase detector circuits, respective ones of the plurality of phase detector circuits being configured to generate respective ones of a plurality of error signals responsive to respective ones of a plurality of clock signals generated by the respective ones of the plurality of clock circuits that are directly connected thereby, the respective ones of the plurality of clock circuits being configured to generate respective ones of the plurality of clock signals responsive to respective ones of the plurality of error signals that are generated by the respective ones of the plurality of phase

> detector circuits that directly connect the respective ones of the plurality of clock circuits to the at least one other of the plurality of clock circuits. (emphasis added)

Independent Claim 14 is directed to method for distributing a clock signal in which both a first and a second clock signal are each generated responsive to an error signal as indicated by the recitations of Claim 14 reproduced in part below:

> generating a first clock signal responsive to an error signal;
> generating a second clock signal responsive to the error signal;
> ... (emphasis added)

Independent Claim 19 is directed to a system for distributing a clock signal that comprises both a means for generating a first clock signal and a means for generating a second clock signal. Both the means for generating the first clock signal and the means for generating the second clock signal are responsive to an error signal as indicated by the recitations of Claim 19 reproduced in part below:

> means for generating a first clock signal responsive to an error signal;
> means for generating a second clock signal responsive to the error signal;
> ... (emphasis added)

Thus, independent Claims 1, 14, and 19 all include recitations that indicate that the first and second clock signals are generated responsive to a common error signal. In sharp contrast, the internal clock signal CLK-I shown in FIG. 3 of Manning is generated responsive to the error signal E output from the phase detector 36, but the external clock signal CLK-E is not generated responsive to the error signal E. Therefore, Manning does not disclose or suggest generating two or more clock signals responsive to a common error signal as recited in independent Claims 1, 14, and 19.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that independent Claims 1, 14, and 19 are patentable over the cited reference and that Claims 1 - 7, 15 - 18, and 20 - 24 are patentable at least per the patentability of independent Claims 1, 14, and 19.

Independent Claim 8 is Patentable

Independent Claim 8 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Manning. Independent Claim 8 is directed to a clock distribution circuit that comprises a plurality of clock circuits that are responsive to respective ones of a plurality of error signals that are generated by respective ones of a plurality of phase detector circuits that directly connect respective ones of the plurality of clock circuits to one or more other ones of the clock circuits as indicated by the recitations of Claim 8 reproduced in part below:

> ...
> a plurality of clock circuits, respective ones of the plurality of clock circuits being directly connected to at least one other of the plurality of clock circuits by respective ones of the plurality of phase detector circuits, respective ones of the plurality of phase detector circuits being configured to generate respective ones of a plurality of error signals responsive to respective ones of a plurality of clock signals generated by the respective ones of the plurality of clock circuits that are directly connected thereby, the respective ones of the plurality of clock circuits being configured to generate respective ones of the plurality of clock signals responsive to respective ones of the plurality of error signals that are generated by the respective ones of the plurality of phase detector circuits that directly connect the respective ones of the plurality of clock circuits to the at least one other of the plurality of clock circuits. (emphasis added)

According to Claim 8, the clock circuits generate the clock signals responsive to error signals generated by phase detectors that connect the clock circuits. In sharp contrast, Manning discloses a single clock generation circuit 34 that is configured to generate an internal clock signal CLK-I that is synchronized with an external clock signal CLK-E. (Manning, FIG. 3). Moreover, Manning explains that the purpose of embodiment described therein is to solve a problem "in high-speed integrated circuits in which an externally applied clock is intended to be registered with other signals present in the integrated circuit. (Manning, col. 1, lines 15 - 19). Manning, therefore, appears to be directed to using a clock generation circuit to synchronize an internally generated clock signal (CLK-I) to an externally generated clock signal (CLK-E). Because the clock signal CLK-E is externally generated, Applicants submit that Manning does not disclose or suggest synchronizing the external clock signal CLK-E

with the internal clock signal CLK-I because the external clock signal CLK-E is not under the control of the integrated circuit. Thus, Applicants respectfully submit that Manning contains no disclosure or suggestion of modifying the clock generation circuit shown in FIG. 3 to use phase detectors to connect clock circuits so as to generate error signals that are used to synchronize the clock signals generated by the clock circuits to each other as recited in independent Claim 8.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that independent Claims 8 is patentable over the cited reference and that Claims 9 - 13 are patentable at least per the patentability of independent Claim 8.

Independent Claims 25 and 26 are Patentable

Independent Claims 25 and 26 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Manning. Independent Claim 25 is directed to a method of distributing a clock signal over an integrated circuit and recites:

> independently generating a plurality of clock signals on the integrated circuit such that respective ones of the plurality of clock signals are distributed to respective portions of the integrated circuit; and
>
> synchronizing phases of the plurality of clock signals to one another.

Independent Claim 26 includes similar recitations. Thus, Claims 25 and 26 describe the independent generation of multiple clock signals on an integrated circuit and synchronizing the phases of the clock signals to one another.

As discussed above with respect to independent Claim 8, Manning describes internally generating a single clock signal on an integrated circuit and synchronizing the phase of the internally generated signal (CLK-I) to an externally generated signal (CLK-E). (Manning, FIG. 3). Manning contains no disclosure or suggestion of synchronizing the phases of multiple clock signals generated internally in the same integrated circuit as recited in Claims 25 and 26.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that independent Claims 25 and 26 are patentable over the cited reference.

Various Dependent Claims are Separately Patentable

With regard to Claim 2, this claim includes all the recitations of independent Claim 1 and is, therefore, patentable over the cited reference for at least the reasons stated above. Applicants further submit, however, that Claim 2 is separately patentable because Manning does not disclose or suggest the recitation "wherein the first clock circuit is further configured to generate the first clock signal responsive to the first and second error signals." Applicants respectfully submit that Manning contains no disclosure or suggestion of generating a clock signal based on multiple error signals. Applicants further submit that Claim 16 is separately patentable for similar reasons.

With regard to Claim 4, this claim includes all the recitations of independent Claim 1 and is, therefore, patentable over the cited reference for at least the reasons stated above. Applicants further submit, however, that Claim 4 is separately patentable because Manning does not disclose or suggest "a summation circuit that is configured to add the first and the second error signals..." as recited in Claim 4. Applicants respectfully submit that Manning contains no disclosure or suggestion of using a summation circuit to add multiple error signals. Applicants further submit that Claim 10, 17, and 22 are separately patentable for similar reasons.

With regard to Claim 5, this claim includes all the recitations of independent Claim 1 and is, therefore, patentable over the cited reference for at least the reasons stated above. Applicants further submit, however, that Claim 5 is separately patentable because Manning does not disclose or suggest a loop filter circuit that comprises a first and second amplifier circuit as recited in Claim 5. Applicants respectfully submit that the loop filter circuit 34 shown in FIG. 3 of Manning does not disclose or suggest multiple amplifier circuits. Applicants further submit that Claim 11 is separately patentable for similar reasons.

With regard to Claim 6 this claim includes all the recitations of independent Claim 1 and is, therefore, patentable over the cited reference for at least the reasons stated above. Applicants further submit, however, that Claim 6 is separately patentable because Manning does not disclose or suggest a phase detector that comprises first and second pulse generator

circuits as recited in Claim 6. Applicants respectfully submit that Manning contains no disclosure with respect to the particular design used in phase detector circuit 36 shown in FIG. 3. Applicants further submit that Claims 12, 18, and 23 are separately patentable for similar reasons.

With regard to Claim 7 this claim includes all the recitations of independent Claim 1 and is, therefore, patentable over the cited reference for at least the reasons stated above. Applicants further submit, however, that Claim 7 is separately patentable because Manning does not disclose or suggest the first clock circuit, the second clock circuit, and the phase detector circuit being contained in a single integrated circuit chip as recited in Claim 7. As discussed above, the external clock signal (CLK-E) is generated external to the integrated circuit 30 where the internal clock signal (CLK-I) is generated. (Manning, FIG. 3). Thus, Manning does not disclose or suggest the first and second clock circuits being contained in a single integrated circuit chip. Applicants further submit that Claims 13 and 24 are separately patentable for similar reasons.

CONCLUSION

In light of the above amendments and remarks, Applicants respectfully submit that the above-entitled application is now in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

Respectfully submitted,

D. Scott Moore
Registration No. 42,011

Customer No. 20792
Myers Bigel Sibley & Sajovec
P. O. Box 37428
Raleigh, North Carolina 27627
Telephone: (919) 854-1400
Facsimile: (919) 854-1401

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Michele P. McMahan